Best Combination Between Power Density, Efficiency, and Gain at V-Band with an InP-Based PHEMT Structure

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***Abstract*— In this letter, we report on the state-of-the-art combination at V-band between simultaneously power density (370 mW/mm), power-added efficiency (28.3%), and power gain (5.2 dB) of InP pseudomorphic HEMT's biased at a low drain voltage of 2 V. The performance of these double delta-doped pseudomorphic AlInAs/GaInAs HEMT's on InP with an original strain compensated channel was measured at 60 GHz. This demonstrates a good potentiality for low-voltage applications in order to reduce the power supply of systems.**

I. Introduction

A LOT of work has been done on InP-based HEMT's for low-noise or low-power applications because they demonstrated higher microwave performance superior than those of any other transistor [1]. In the case of low noise, many devices have been realized with a lattice-matched channel, allowing a high conduction band discontinuity at the InGaAs/InAlAs heterostructure interface, an excellent electron mobility, and peak velocity in the InGaAs channel [2]. These advantages can be improved by increasing the indium mole fraction [3]. In the case of power amplifiers, high breakdown voltages are more crucial than for low-noise amplifiers. That is why many authors have reported structures where the channel is often lattice matched [4], [5] and the aluminum fraction in the barrier is increased. To our knowledge, the best result in term of output power with an InP-based HEMT at around 60 GHz has been obtained by Matloubian *et al.* [4] with an output power of 180 mW (400 mW/mm), a power-added efficiency (PAE) of 27%, and 3-dB gain at 3.5-V drain-to-source voltage.

However, in the case of low-supply applications, the dc bias is limited [6]. Hence, to obtain high power density, it is necessary to achieve high current density. For this reason, in this work we report the fabrication and measurements of an original InP power PHEMT with a strain-compensated channel and two delta-doped planes in order to reach a very high current density. A high aluminum fraction in the barrier has also been inserted to increase the conduction band discontinuity. Power measurements at 60 GHz represent to our knowledge the best combination between a power density of 370 mW/mm, a PAE of 28.3%, and power gain of 5.2 dB.

Manuscript received August 4, 1997. This work was supported by the French MOD (DGA).

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Publisher Item Identifier S 1051-8207(98)00862-9.

II. Device Design

To achieve high current densities with power HEMT's, we have used, an original strain-compensated layer. A cross section of the power HEMT considered is shown in Fig. 1. The layers were grown by molecular beam epitaxy on a semi-insulated InP substrate. The buffer consists of a 100-nm AlInAs layer and a 300-nm-thick AlInAs layer grown at low temperature (400 °C). The active part of the structure is a 15-nm $Ga_{0.35}In_{0.65}As$ pseudomorphic channel with two 5-nm AlInAs spacer layers on both side of the channel. The bottom AlInAs layer is lattice matched with a δ-doped plane at 2×10^{12} cm^{-2}. To improve the Schottky-barrier height of the gate, a 15-nm undoped pseudomorphic $Al_{0.65}In_{0.35}As$ layer with a δ-doped plane of 4×10^{12} cm^{-2} was grown. Finally, a 7-nm doped (5×10^{18} cm^{-3}) GaInAs layer was grown to facilitate ohmic contact formation. The two-dimensional electron gas (2-DEG) was formed in the pseudomorphic GaInAs channel by electron transfer from silicon δ doping above and below the AlInAs layer. The dual δ-doped structure provides high carrier concentration in the channel and leads to a high current density which benefits the power device performance. Hall measurements indicate, at room temperature, an electron sheet charge density of 4.6×10^{12} cm^{-2} with an approximate mobility of 15 000 cm^2/V·s. The fabricated device has a total gate width of 2×50 μm with a 0.25-μm gate length.

III. Device Performance

These InP HEMT's have demonstrated a peak transconductance Gm of 800 mS/mm. They exhibit a full channel current $I_{\max}$ of 1480 mA/mm (defined as the drain saturation current density measured at a gate-to-source voltage of 0.6 V) measured at a drain to source voltage of 2 V. The gate-to-drain or gate-to-source diodes breakdown voltages measured at 1 mA/mm of gate current are 4.5 V. The turn-on voltage and the pinch-off voltage are, respectively, 0.9 and -2.5 V.

S-parameter measurements of the devices were performed from 0.5 to 75 GHz using automatic network analyzers. An intrinsic current gain cutoff frequency (F_T) of 105 GHz and a maximum available gain of 10 dB at 60 GHz have been obtained at a drain bias of 2 V. The power performance of the HEMT were measured at 60 GHz using an on wafer probe system. Mechanical tuners were adjusted to obtain maximum output power and minimum reflected input power.

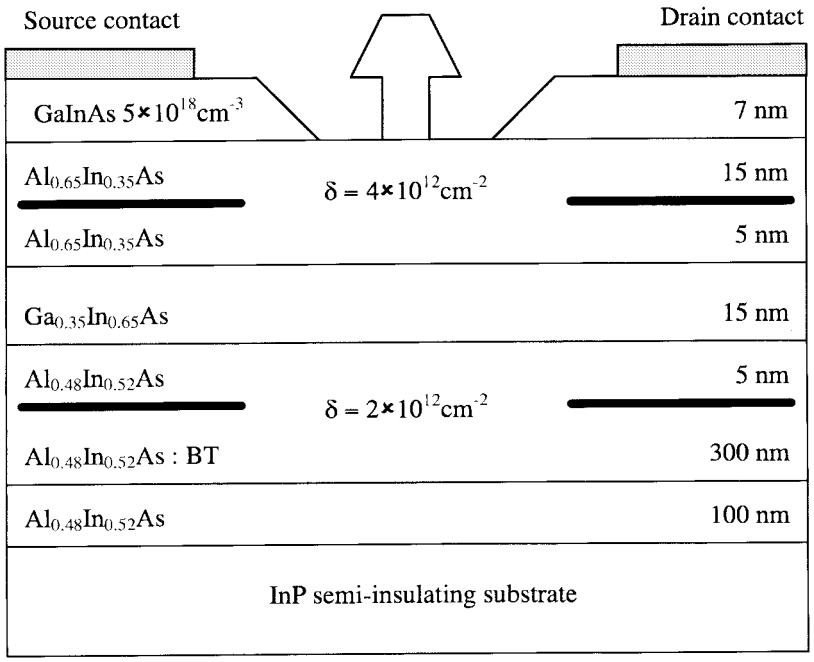

Fig. 1. Cross section of the double δ-doped pseudomorphic $Al_{0.65}In_{0.35}As$/ $Ga_{0.35}In_{0.65}As$/InP HEMT.

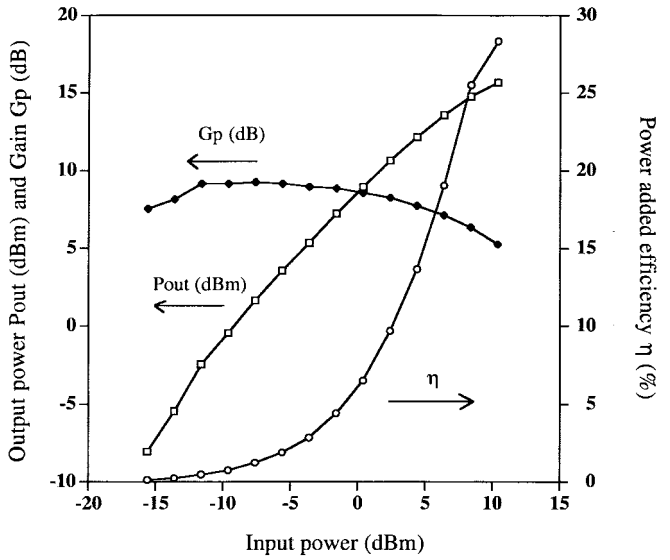

Fig. 2. Power characteristics at 60 GHz for the following bias conditions: $V_{ds} = 2$ V and $V_{gs} = -1.5$ V.

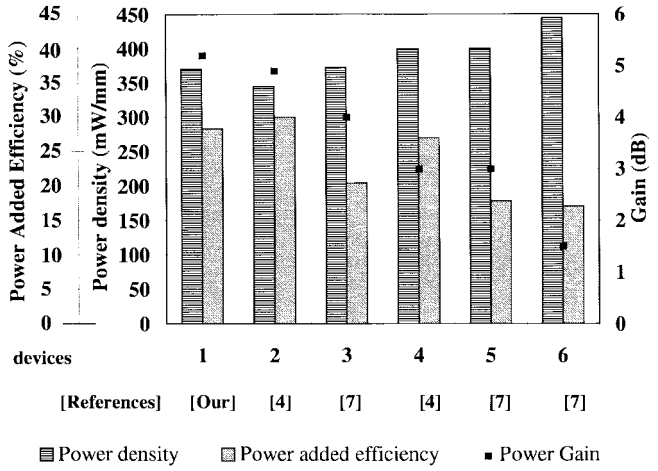

Fig. 3. Comparison of the state-of-the-art power density, PAE, and power gain on discrete devices at about 60 GHz on InP.

The measured input and output power were corrected in order to take into account the losses of the probes and the waveguide. The measured power performance of devices biased at a V_{ds} of 2 V and V_{gs} of -1.5 V to operate in class A are shown in Fig. 2. They have demonstrated a maximum output power of 15.7 dBm corresponding to a power density of 370 mW/mm with a PAE of 28.3% and 5.2-dB gain. In order to compare our results with other power devices at 60 GHz on InP HEMT, we report Fig. 3 a graph with the most significantly published results. Even if our devices exhibit a power density slightly inferior to the other, it seems to be the best compromise between the three items: power density, gain, and efficiency. We have obtained less power density but much more PAE and gain than devices numbered 3, 4, 5 and 6. The devices numbered 2 have a slightly better PAE (30%) than our devices but a gain and power density inferior. That is why we can consider that, to our best knowledge, we have achieved the state-of-the-art combination between simultaneously power density, PAE, and power gain.

The fabricated double δ-doped HEMT has demonstrated good potentiality for low-voltage operation in power conditions. The reduction of the power consumption of circuits allows to decrease the number of the battery cells and then to the reduction of the size and weight of systems.

IV. Conclusion

In this letter, we report on state-of-the-art combination between power density, PAE, and power gain on original InP PHEMT's with a strain compensated layer. Power measure-

ments at 60 GHz have given a power density of 370 mW/mm with a PAE of 28.3% and 5.2-dB gain at a low drain-to-source voltage of 2 V. These devices exhibit a current density as high as 1480 mA/mm. They have demonstrated a good potentiality for low-voltage operation in order to reduce the power consumption of systems. By further optimization of the gate recess dimensions and also incorporating a 0.15-μm gate length in our power PHEMT's, we expect some improvement of the power performance of these transistors in V-Band.

ACKNOWLEDGMENT

The authors would like to acknowledge M. Zaknoune for his helpful discussions and F. Diette for device processing.

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